WHAT IS CLAIMED IS:

1. A method for converting serial data to parallel data, the method comprising:

serially loading bits of data into a first register in response to a first periodic signal;

parallel loading bytes of the data from the first register into a second register in response to a second periodic signal; and

changing boundaries between the data bytes in response to a third signal.

2. The method of claim 1 wherein changing the boundaries between the data bytes in response to a the third signal further comprises changing the phase of the second periodic signal in response to the third signal, wherein the change in the phase of the second periodic signal causes one of the bits of the data stored in the first register to be discarded.

3. The method of claim 1 further comprising:

parallel loading the data bytes from the second register into a third register.

4. The method of claim 3 further comprising:

generating fourth and fifth periodic signals, wherein the third register synchronizes the data bytes to the fourth periodic signal in response to the fifth periodic signal, and wherein the fourth periodic signal is used as a clock signal by core circuitry that receives the data from the third register.

5. The method of claim 3 further comprising:

parallel loading the data bytes from the third register into core circuitry of a programmable logic device.

6. The method of claim 1 further comprising:

generating the first periodic signal using a phase lock loop; and

providing the first periodic signal to an input of a first counter, wherein the first counter generates the second periodic signal.

7. The method of claim 6 further comprising:

parallel loading the data bytes from the second register into a third register; and

providing the first clock signal to an input of a second counter, wherein the second counter generates a fourth periodic signal that controls when the data bytes are loaded into the third register.

8. The method of claim 1 further comprising:

disabling the third signal to prevent the boundaries between the data bytes from changing.

9. The method of claim 1 wherein changing the boundaries between the data bytes in response to the third signal further comprises realigning a data boundary between bytes of the data bytes by one bit in response to the second periodic signal.

10. The method of claim 9 wherein changing the boundaries between the data bytes in response to the third signal further comprises realigning a data boundary between bytes of the data bytes by two bits in response to the second periodic signal.

11. A serial-to-parallel data conversion circuit comprising:

a first register coupled to receive serial data;

a second register coupled to receive parallel data bytes from the first register; and

a first counter circuit providing a first periodic signal that controls when the parallel data bytes are transferred from the first register to the second register, the first periodic signal causing boundaries between the parallel data bytes to change in response to a second signal.

12. The serial-to-parallel data conversion circuit of claim 11 further comprising:

a phase locked loop circuit that provides a third periodic signal to the first and second registers and to the first counter, wherein data is shifted through the first and second registers in response to the third periodic signal.

13. The serial-to-parallel data conversion circuit of claim 11 further comprising:

a third register coupled to receive the parallel data bytes from the second register; and

a second counter circuit providing a third periodic signal that controls when the parallel data bytes are transferred from the second register into the third register.

14. The serial-to-parallel data conversion circuit of claim 13 wherein the third register synchronizes the parallel data to a fourth periodic signal generated by the second counter.

15. The serial-to-parallel data conversion circuit of claim 13 further comprising:

a fourth register coupled between the first counter and the second register; and

a fifth register coupled between the second counter and the third register.

16. The serial-to-parallel data conversion circuit of claim 11 further comprising:

a third register coupled to the first counter, the third register generating the second signal, wherein an input of the third register is coupled to receive a fourth signal that blocks the second signal.

17. A method for converting serial data to parallel data, the method comprising:

loading bits of the serial data into a first data storage circuit in response to a first periodic signal;

loading the bits from the first data storage circuit into a second data storage circuit as parallel data bytes in response to a second periodic signal, wherein boundaries between the parallel data bytes are determined by the second periodic signal; and

shifting the boundaries between the parallel data bytes in response to a third signal.

18. The method of claim 17 wherein shifting the boundaries between the parallel data bytes in response to the third signal further comprises increasing the period of the second periodic signal in response to the third signal.

19. The method of claim 17 further comprising:

loading the parallel data bytes from the second data storage circuit into a third data storage circuit; and

generating a fourth periodic signal that controls when the data bytes are loaded into the third data storage circuit.

20. The method of claim 17 further comprising:

generating the first periodic signal using a phase lock loop; and

providing the first periodic signal to an input of a first counter, wherein the first counter generates the second periodic signal.

21. The method of claim 17 further comprising:

disabling the third signal to prevent the boundary between parallel data bytes from shifting.

22. A serial-to-parallel data converter comprising:

means for storing bits of serial data in a first storage circuit;

means for storing the bits as parallel data bytes in a second storage circuit;

means for providing a first periodic signal that controls when the bits are transferred from the first storage circuit to the second storage circuit; and

means for providing a second signal to the means for providing the first periodic signal, wherein the first periodic signal causes a boundary between the parallel data bytes to change by at least one bit in response to the second signal.

23. The serial-to-parallel converter of claim 22 further comprising:

means for storing the parallel data bytes in a third storage circuit; and

means for providing a third periodic signal that controls when the parallel data bytes are transferred from the second storage circuit to the third storage circuit.

24. The serial-to-parallel converter of claim 22 further comprising:

means for generating a third periodic signal using a phase locked loop, wherein the third periodic signal is provided to the first and the second storage circuits and to the means for providing the first periodic signal.